CLAIMS

What is claimed is:

1. A method of fabricating copper metallization on backside of GaAs devices, comprising:

   a substrate, thereon via holes are fabricated ;

   a diffusion barrier layer formed on said backside of said substrate; and

   a copper metallization layer formed on said barrier layer.

2. A method as claimed in claim 1, wherein said substrate is made of gallium arsenide (GaAs).

3. A method as claimed in claim 1, wherein said via holes can be fabricated by etching through a use of inductively coupled plasma (ICP).

4. A method as claimed in claim 1, wherein said diffusion barrier layer can be deposited by sputtering on said backside of said substrate.

5. A method as claimed in claim 1, wherein said diffusion barrier layer can be deposited by evaporating on said backside of said substrate.

6. A method as claimed in claim 1, wherein said diffusion barrier layer has a thickness of 40 to 100 nm.

7. A method as claimed in claim 1, wherein said diffusion barrier layer can be a thin film of tungsten (W).

8. A method as claimed in claim 1, wherein said diffusion barrier layer can be said thin film of tungsten nitride (WN).

9. A method as claimed in claim 1, wherein said diffusion barrier layer can be said thin film of titanium tungsten nitride (TiWN).

10. A method as claimed in claim 1, wherein said copper metallization layer can be deposited by said sputtering on said diffusion barrier layer.

11. A method as claimed in claim 1, wherein said copper metallization layer can be deposited by said evaporating on said diffusion barrier layer.

12. A method as claimed in claim 1, wherein said copper metallization layer can be deposited by electroplating on said diffusion barrier layer.

13. A method as claimed in claim 1, wherein said copper metallization layer has a thickness of 2 to 10 μm.